Design of Frequency Synthesizer Based on Wireless Communication Network

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Abstract: The basic composition and design principle of the frequency synthesizer are introduced, and the theoretical analysis of each component is carried out, and the specific design scheme and implementation method on the basis of wireless communication are given. The simulation results show that the design is simple and reasonable, flexible and convenient, with good cost performance, and can be applied to various digital receiving systems.

1. Introduction

The frequency synthesizer is a new type of frequency synthesizer which synthesizes the phase directly, which is far superior to the traditional frequency synthesizer in relative bandwidth, frequency conversion time, orthogonal output, phase continuity, frequency resolution and other performance indicators. At present, there are many kinds of frequency synthesizer chips available in the market, but these special chips have high cost and some defects in flexibility. Therefore, it is necessary to design a frequency synthesizer to meet your own needs by using high-performance wireless communication.

2. Principle of Frequency Synthesizer

As shown in Figure 1, the main function of frequency synthesizer is to generate a sine wave

$$S(n)=\cos(2\pi f_0 n / f_s) \tag{1}$$

In which, f_0 is the frequency of the input IF signal; f_s is the sampling frequency.

The frequency synthesizer is mainly composed of phase accumulator, quantizer, lookup table, scrambler, etc. The functions of each part are as follows:

Phase accumulator: converts the digital local frequency into phase, and accumulates one phase increment for each clock pulse;

Quantizer: truncates the accumulated phase value reasonably and converts it to the input address of the lookup table, so as to effectively reduce the depth of the lookup table;

Lookup table: corresponds the phase address with the sine value one by one, and output the sine signal required;

Scrambler: adds noise into the accumulated phase value to eliminate the resonance error added by the accumulator.

3. Design and Analysis of Frequency Synthesizer

(1) Phase accumulator. A phase increment $\Delta\theta = 2\pi f_0 / f_s$ is added to the input phase of each clock pulse. If $B_{\theta(n)}$ is used to signify the width of the phase accumulator, f_{out} signifies the output frequency, $\Delta\theta$ signifies the phase increment and Δf signifies the frequency resolution, the relationship between them can be expressed as

$$f_{out}=\frac{f_s \Delta\theta}{2B_{\theta(n)}} \tag{2}$$

$$\triangle f = \frac{f_s}{2B_{\theta(n)}} \tag{3}$$

Because frequency conversion speed is one of the most important indexes of frequency synthesizer, the design of this part adopts the method of combining carry chain and pipelining technology, which both improves the utilization of chip resources, and the performance and speed of the system on.

(2) Quantizer. Due to the high frequency resolution usually required, according to formula (3), $B_{\theta(n)}$ is relatively larger. For instance, under the sampling frequency of 180 MHz, if the frequency accuracy is 1 Hz, and then $B_{\theta(n)}$ = 28bits. If it is directly used as the lookup table address, then the ROM required is very large. Since the ram integrated in the current wireless communication is limited, it is necessary to use off-chip RAM, which will increase the complexity of the system. Therefore, a quantizer Q is added to the design, the function is to convert the accumulated phase $\theta(n)$ to address $\Theta(n)$ as the address input of look-up table T. If $B_{\Theta(n)}$ is used to signify the width of look-up table address and SFDR to signify the spurious free dynamic range (dB), then

$$B_{\Theta(n)} \geq \left[\log_2 \frac{SFDR}{6} \right] \tag{4}$$

The equation (4) shows that SFDR can be increased by about 6 dB for each bit of increase in the width of lookup table address.

(3) Look-up table. The look-up table reads out the sine wave of the required frequency one by one according to the address of the sample pre-existing in RAM.The look-up table has two key parameters, one is the depth of the look-up table, which is determined by $B_{\Theta(n)}$. According to the sine wave symmetry, only 1 / 4 cycle waveform needs to be stored in RAM, thus the depth of the look-up table should be $2B_{\Theta(n)} - 2$; the other is the length of each data B_{out} in the look-up table. In order to prevent "passivation" phenomenon, it should meet the following formula

4. Design and Simulation of Frequency Synthesizer Based on Wireless Communication

Wireless communication (field programmable gate array) is a kind of programmable logic device whose gate circuit can reach millions and clock frequency can reach hundreds of megabytes. Taking Virtex II of Xilinx company as an example, its basic composition is configurable logic module (CLB), each CLB is composed of two slices, each slice contains a four input look-up table (LUT),together with a carry logic and a trigger. In the meantime, different types of chips also integrate multipliers, ram sand other resources in different quantities.

The receiver of the small aircraft measurement and control system requires the basic parameters of the frequency synthesizer: the system clock is 180 MHz (i.e. the sampling rate of the output waveform); the frequency resolution is 1 Hz; SFDR = 68dB; the output frequency is 70 MHz; the output data width is 12 bits. After the calculation, the required ram size is 1K × 12bits, and other functions need to be integrated in the same EPGA. Therefore, XC2V1000 of Virtex II series of Xilinx company is selected as the hardware development platform. The chip has a capacity of 40 × 32 CLB (configurable logic block), 40 multiplication modules and a maximum of 720kb BlockRam. This design uses on-chip integrated block BlockRam, uses core generator 6.1.03i tool of Xilinx company to call RAM resources on the chip, and inputs sine wave through Memory Editor, which greatly facilitates the design process. During the preliminary synthesis in ISE6. 1 of Xilinx company , 90 look-up tables (about 23 CLBs), 190 REG and 1 blockram were used.

In the process of development, VHDL language was used, Modelsim SE 5. 7g of Mentor Graphic company was used for simulation and emulation, Synplify Pro7.2 of Synplicity company was used as the synthesis tool, and ISE6. 1 of Xilinx company was used for wiring and downloading.

The conditions without and with the scrambler were simulated respectively, two sets of data in

Modelsim were obtained and the results acquired is as shown in Figure. 2. The circuit timing chart and data added with scrambling were acquired.

From the simulation results, it can be clearly seen that although the quantizer Q effectively reduced the depth of the look-up table under the premise of ensuring the SFDR unchanged, it introduced the resonance error. After adding the scrambler D, on the one hand, the resonance error was eliminated, on the other hand, the depth of the look-up table was further reduced without affecting the SFDR.

5. Conclusion

The frequency synthesizer has been used and tested in the above digital receivers, and the test results are in good agreement with the simulation results. Since it can change the parameters at any time according to the needs of different applications, it can be widely applied in the digital receiver of other measurement and control systems.

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